Multicore software development
Platform architectures and patterns
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TP4 Industrial Platforms for Multicore Systems

Development and extension of established industrial platforms for the use in multicore based systems

Investigation of basis software, middleware and operating systems

Evaluation and development of fail-operational concepts for multicore platforms
TP4 Industrial Platforms for Multicore Systems

Automotive

Avionics

Industry Automation
TP4 Industrial Platforms for Multicore Systems

Consortium

Automotive
- Audi
- Continental
- BOSCH
- SCHAEFFLER
- LUK
- FAG
- DENSO

Avionics
- AIRBUS
- General Electric (GE)
- HENSOLDT
- DIEHL Aerospace
- LIEBHERR Engines

Software & Tool Vendors
- AbsInt
- Timing Architects
- SYMTA VISION
- SILEXICA
- Opensynergy

Industry Automation
- WIKA Mobile Control
- VECTOR
- SYSGO Embedded Innovations
- SIEMENS

Research-organizations
- DLR
- Technische Universität Braunschweig
- Fraunhofer
- KIT
- CAU Universität Kiel
- TUM Technische Universität München
- Fortiss Institute for Systems Integration

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Platform architecture and distribution patterns

- MIDDLEWARE
  - HIERARCHICAL SCHEDULING
  - VIRTUALIZATION & HYPERVERSORS
- COMMUNICATION
- CODE QUALITY
- BSW DISTRIBUTION

Synchronization and Communication

- RESOURCE BROKERING
  - MIXED CRITICALITY
  - QUALITY-OF-SERVICE
  - TIME DIVISION MULTIPLEXING
  - REAL-TIME
  - RELIABILITY
  - NETWORK ON CHIP

Fail-operational concepts

- FAILURE MODES
  - SWITTOVER MECHANISMS
  - ISO 26262
  - FAILURE DIAGNOSIS
  - SIMPLEX ARCHITECTURE
  - REDUNDANCY
  - FAULT TOLERANCE
• Parametric runtime environment

• Master-satellite pattern

• Hierarchical scheduling

• Task management in heterogeneous systems
• Communication layer for networks-on-chips
• Communication semantics and model transformation
• Inter-processor communication in heterogeneous architectures
• Fault tolerant communication
• Communication with low latency and real-time requirements
Virtualization concepts and hypervisor implementation

Virtualization of heterogeneous systems

Online-monitoring of hypervisor operation

Embedded hypervisor
• Safety assurance and contract based design
• Hypervisor code quality
• Isolated and protected channels inside a chip
• Dynamic migration of functions for heterogeneous SoCs
• Fail-operational switchover mechanisms
• Efficient fail operational multicore processor
• Fail operational concepts for NoC-based multicore systems
• Threat models and mitigation
• Isolated and protected channels inside a chip
• Secure interface to modules outside of a chip
Conclusion

• Successful collaboration between industrial partners and research organizations

• Several scientific publications

• Validation of platform solutions in demonstrators
Thank you for your attention!

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